**D1D1D1D1D1D1D1D1D1D1D1D1D1D1D1D**

**Computer Architecture**

**Quiz No. 2, Fall 2019 Std. No. \_\_\_\_\_\_\_\_**

**Q1:** What is the clock frequency of a pipelined processor having four stages with the following delays: S1 = 25nSec; S2 = 15nSec; S3 = 30nSec and S4 = 15nSec? The pipeline latch delay is 2nSec. (1.5)

**Q2:** What are the operations performed in the ID stage of RISC V integer pipeline? (1.5)

**Q3:** What are data hazards? (1)

**Q4:** Which exception is the most difficult to handle in pipelined processors and why? (2)

**Q5:** What is meant by loop-level parallelism? (1.5)

**Q6:** Differentiate between synchronous and asynchronous exceptions. (1.5)

**Q7**: Why are WAR and WAW hazards referred to as name dependence? (1)

**D2D2D2D2D2D2D2D2D2D2D2D2D2D2D2D**

**Computer Architecture**

**Quiz No. 2, Fall 2019 Std. No. \_\_\_\_\_\_\_\_**

**Q2:** What are the operations performed in the EX stage of RISC V integer pipeline? (1.5)

**Q1:** What is the clock frequency of a pipelined processor having four stages with the following delays: S1 = 22nSec; S2 = 10nSec; S3 = 32nSec and S4 = 12nSec? The pipeline latch delay is 2nSec. (1.5)

**Q3:** What are control hazards? (1)

**Q5:** What is meant by loop-level parallelism? (1.5)

**Q4:** What are precise exceptions? (1.5)

**Q6:** Differentiate between user requested and coerced exceptions. (1.5)

**Q7**: How does register renaming help overcome WAR and WAW hazards? (1.5)

**F1F1F1F1F1F1F1F1F1F1F1F1F1F1F1F1F1**

**Computer Architecture**

**Quiz No. 2, Fall 2019 Std. No. \_\_\_\_\_\_\_\_**

**Q1:** What is the speedup of a pipelined machine over its non-pipelined counterpart, if the 4-stage pipelined processor has the following delays: S1 = 30nSec; S2= 20nSec; S3 = 18nSec, and S4 = 15nSec? There is a pipeline latch delay of 2nSec. (2)

**Q2:** Differentiate between static and dynamic branch prediction techniques. (1.5)

**Q3:** Why are dynamic pipeline scheduling more effective than static scheduling? (1.5)

**Q4:** How is internal forwarding implemented in Tomasulo’s approach of pipeline scheduling? (1.5)

**Q5:** When does an imprecise exception occur? (1.5)

**Q6:** What are the limitations of a Scoreboard that has been overcome is Tomasulo’s approach? (2)

**F2F2F2F2F2F2F2F2F2F2F2F2F2F2F2F2F2**

**Computer Architecture**

**Quiz No. 2, Fall 2019 Std. No. \_\_\_\_\_\_\_\_**

**Q1:** What is the speedup of a pipelined machine over its non-pipelined counterpart, if the 4-stage pipelined processor has the following delays: S1 = 25nSec; S2= 20nSec; S3 = 18nSec, and S4 = 20nSec? There is a pipeline latch delay of 2nSec. (2)

**Q2:** Why are dynamic pipeline scheduling more effective than static scheduling? (1.5)

**Q3:** Differentiate between static and dynamic branch prediction techniques. (1.5)

**Q4:** How is internal forwarding implemented in Tomasulo’s approach of pipeline scheduling? (1.5)

**Q5:** What are the limitations of a Scoreboard that has been overcome is Tomasulo’s approach? (2)

**Q6:** When does an exception become imprecise? (1.5)